4 4
t_7

Hall Ticket No.:

Course Code: 23MTVLE01

MALINENI LAKSHMAIAH WOMEN'S ENGINEERING COLLEGE (AUTONOMOUS)

I - M.Tech. I - Semester (MR23) Regular Examinations, March - 2024

VLSI TECHNOLOGY

Department of Electronics & Communication Engineering

Time: 3 hours Max. Marks: 75

Answer **ALL** the questions – **5*15=75 Marks**

Q. No.		Question	Marks	СО	BL
	a)	Derive I _{ds} -V _{ds} relationship of MOS Transistor in Resistive region?	8M	CO1	L3
1	b)	Derive an expression for trans-conductance of an n-channel enhancement MOSFEToperating in active region?	7M	CO1	L3
(OR)					
	a)	What is difference between enhancement type and depletion type MOSFETs? Explain why enhancement type MOSFET is preferred?	8M	CO1	L4
2	b)	Consider an N-MOSFET as shown in figure below. What will be the change in I_D if V_{DD} changesfrom 3.3 to 1.8V.Consider VTH=0.5V and $\mu_N C_{OX}$ W/L=100 $\mu A/V^2$.	7M	CO1	L5

3	а	What are the steps involved in CMOS n-Well Fabrication? Explain with neat sketches.	8M	CO2	L3
	b	What is meant by latch up? How can it be eliminated?	7M	CO2	L4
(OR)					
4	а	Determine the pull up to pull down ratio for NMOS inverter driven byanother NMOS inverter?	8M	CO2	L3
	b	Analyze CMOS inverter with its transfer characteristics?	7M	CO2	L4

5	а	Draw the schematic diagram, stick diagram and layout of 2-input CMOS NAND	8M	СОЗ	L4
	b	Explain 2 µm Double Metal, Double Poly CMOS / Bi-CMOS Rules?	7M	CO3	L4
(OR)					
6	а	What is the need of scaling in MOS circuits? Derive the Scaling factors for MOS transistorparameters?	8M	СОЗ	L4
	b	Draw a stick diagram and layout for CMOS logic Y= (A+B+C)'?	7M	CO3	L5

7	а	Give the design rules for the following cases with neat sketches: (i) Polysilicon – polysilicon (ii) n-type diffusion – n-type diffusion (iii) n-type diffusion – p-type diffusion (iv) metal 1 – metal 2	8M	CO4	L3
		Explain the switch logic and give an example for each one?	7M	CO4	L3
(OR)					
8	а	Derive the expression for CMOS inverter delay in terms of rise time and fall time?	8M	CO4	L3
	b	Explain about the following types of faults with suitable example: (i) Stuck at faults (ii) Bridge faults (iii) Temporary faults	7M	CO4	L3
9	а	Discuss about switching power dissipation and short circuit power dissipation in detail?	8M	CO5	L4
	b	Draw the VLSI design flow diagram and explain?	7M	CO5	L5
(OR)					
10	а	Explain the different categories of DFT techniques?	7M	CO5	L3
10					

Write a short note on low power SRAM technologies?